Infinity Series H.100 Loop Start Board

TECHNICAL MANUAL

Documentation Revision 1.1: Jan. 28, 2011

257M030A

This manual applies to the H.100 PCI version with the 386 processor, the H.100 PCI version with the ARM processor, and the H.100 PCI Express version with the ARM processor. Because of the difference between the processors, there are minor differences in the firmware. These differences have been noted where appropriate.

Note that this manual refers to boards with voice resources. As this firmware is designed to run on boards with a different processor and switching hardware than earlier versions, some sections do not apply to earlier boards. Also note, that the switching chip on the 386 version is different than on the ARM boards which effects some diagnostics.

Contents

Infinity Series H.100 Loop Start Board Technical Manual

American Tel-A-System, Inc.
800-356-9148
• 4800 Curtin Drive • McFarland, WI 53558 •
• 4145 North Service Road, Suite 200 • Burlington, Ontario L7L 6A3 •
• 257M030A•

FCC Part 15 Requirements

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

FCC Part 68 Registration

This equipment complies with Part 68 of the FCC rules and the requirements adopted by the ACTA. On the rear of this board is a label that contains among other information, a product identifier in the format US:AAAEQ##XXXX. If requested, this number must be provided to the telephone company.

This equipment is registered with the FCC under Part 68 as a component device for use with any generic PC Type computer or compatible. In order for FCC registration of this product to be retained, all other products used in conjunction with this product to provide your telephony function must also be FCC Part 68 registered for use with these hosts. If any of these components are not registered, then you are required to seek FCC Part 68 registration of the assembled equipment prior to connection to the telephone network. Part 68 registration specifies that you are required to maintain the approval and as such become responsible for the following:

- any component device added to your equipment, whether it bears component registration or not, will require that a Part 68 compliance evaluation is done and possibly that you have testing performed and make a modification filing to the FCC before that new component can be used;

- any modification/update made by a manufacturer to any component device within your equipment, will require that a Part 68 compliance evaluation is done and possibly that you have testing performed and make a modification filing to the FCC before the new component can be used;

- if you continue to assemble additional quantities of this compound equipment, you are required to comply with the FCC's Continuing Compliance requirements.

The network Interface Jack for this equipment is an RJ21C.

If this XDS H.100 Loop Start Board causes harm to the network, the telephone company will notify you in advance that temporary discontinuance of service may be required. But if advanced notice isn't practical, the telephone company will notify

the customer as soon as possible. Also, you will be advised of your right to file a complaint with the FCC if you believe it is necessary.

The telephone company may make changes in its facilities, equipment, operations or procedures that could affect the operation of the equipment. If this happens the telephone company will provide advanced notice in order for you to make necessary modifications to maintain uninterrupted service.

In case of trouble, you may be required to disconnect the board from the telephone lines until the problem is resolved.

If trouble is experienced with this XDS Loop Start Board, for warranty or repair information please contact:

American Tel-A-System, Inc.
800-356-9148
4800 Curtin Drive
McFarland, WI 53558

If the equipment is causing harm to the telephone network, the telephone company may request that you disconnect the equipment until the problem is resolved.

There are no user serviceable components on the board. All repairs should be accomplished by returning the board to Amtelco with a description of the problem.

Connection to party line service is subject to state tariffs. Contact the state public utility commission, public service commission or corporation commission for information.

If your premise has specially wired alarm equipment connected to the telephone line, ensure the installation of this XDS Loop Start Board does not disable your alarm equipment. If you have questions about what will disable alarm equipment, consult your telephone company or qualified installer.

Connection to telephone company coin service is prohibited.

WARNING: This device contains Electrostatic Sensitive Devices. Proper care should be taken when handling this device to avoid damage from static discharges.

Product Safety

The PSTN cord(s) and telephony power supply must remain disconnected from the telecommunications system until the card has been installed within a host which provides the necessary protection of the operator.

If it is subsequently desired to open the host equipment for any reason, the PSTN cord(s) and telephony power supply must be disconnected prior to effecting access to any internal parts which may carry telecommunications network voltages.

Canadian Customers
CP-01, Issue 8, Part 1
Section 14.1

Notice: "The industry Canada label identifies certified equipment. This certification means that the equipment meets certain telecommunications network protective, operational and safety requirements as prescribed in the appropriate Terminal Equipment Technical Requirements document(s). The Department does not guarantee the equipment will operate to the user's satisfaction.

Before installing this equipment, users should ensure that it is permissible to be connected to the facilities of the local telecommunications company. The equipment must also be installed using an acceptable method of connection. The customer should be aware that compliance with the above conditions may not prevent degradation of service in some situations.

Repairs of certified equipment should be coordinated by a representative designated by the supplier. Any repairs or alterations made by the user to this equipment, or equipment malfunctions, may give the telecommunications company cause to request the user to disconnect the equipment.

Users should ensure for their own protection that the electrical ground connections of the power utility, telephone lines and internal metallic water pipe system, if present, are connected together. This precaution may be particularly important in rural areas.

CAUTION: Users should not attempt to make such connections themselves, but should contact the appropriate electric inspection authority, or electrician, as appropriate.

The PC chassis containing this device shall be placed in a secured location with access restricted to qualified service personnel.

European Approvals

CE Approval

CE

EN55022 EMC declaration

This is a class B product. In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate measures.

No changes or modifications to the H.100 Loop Start card are allowed without explicit written permission from American Tel-A-Systems, Inc., as these could void the end user's authority to operate the device.

Notice: The PC chassis containing this device shall be placed in a secure location with access restricted to qualified service personel.

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1.0 Introduction

The Infinity Series H.100 Loop Start Board is designed to provide twenty-four Loop Start interfaces (twelve without the mezzanine board) connected to the H.100 bus on a board with the PCI bus form factor. Each interface or port provides support for basic line functions such as line seizure, ring detection, and loop current detection. The board is equipped with DSP resources to provide tone generation and detection as well as the detection of Caller ID information. Each port can be programmed to conform to various national standards and practices.

There is a version of the board in both the PCI and PCI Express form factor. This manual covers both versions. For the purposes of this manual, the PCI and PCI Express busses will be referred to as the PCI bus except where it is important to differentiate between them. This manual also is applicable to an earlier version of the board with an Intel 386 processor and voice resources except as noted.

The H.100 bus was devised by the Enterprise Computer Telephony Forum (ECTF) to provide a single telecom bus for the entire industry. It is intended for add-in boards using the PCI form factor. A wide variety of boards are available from a number of different vendors. The H.100 bus also has compatibility modes that allow for connection to legacy computer telephony busses such as the MVIP-90 bus and SCbus.

The board is equipped with a processor that can be used to control the lower level functions of the board. The host PC controls the board using messages passed through dual-ported RAM. The board shares a common message passing and control scheme with other Infinity Series H.100 boards. This scheme is also compatible with legacy XDS boards for the MVIP-90 bus and SCbus.

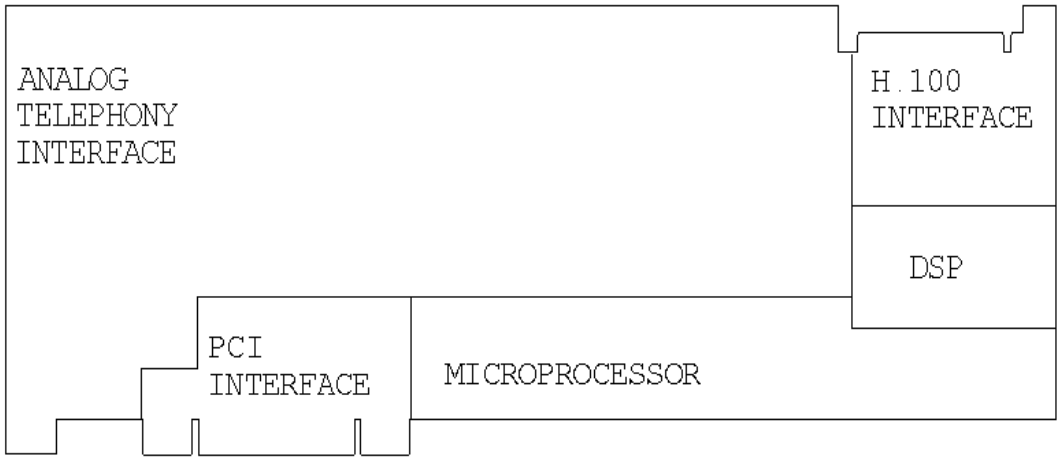

Figure 1: The H.100 Loop Start Board Functional Areas

1.1 Features and Capabilities

This section presents an overview of the features and capabilities of the Infinity Series H.100 Loop Start Board.

1.1.1 The Loop Start Interface

Twenty-four independent ports are provided on the board (twelve without the mezzanine board). Each port on the board provides a complete loop start interface. This includes the ability to seize the line, detect the presence or absence of loop current, and detect ringing signals with a variety of frequencies and cadences. Port timing and impedance characteristics can be set to adapt to different national standards.

1.1.2 Caller Identity

Each port is capable of generating and detecting all the signals necessary for Calling Number Delivery and Calling Name Delivery. Calling Identity Delivery on Call Waiting feature is also supported. All timing is done internally on the board without requiring host intervention.

1.1.3 DSP Functions

The H.100 Loop Start Board is equipped with DSP's that perform a variety of functions. DTMF and Energy detectors are available for each port. DTMF generators are available for each port for signaling purposes. Call Progress tones are also available, with dial-tone, busy, reorder, and audible ringback being provided as well as silence and a 1004 Hz. calibration tone. European call progress tones are also available. In addition, the DSP has voice record and playback capabilities which are beyond the scope of the document.

1.1.4 The H.100 Bus

The H.100 bus is a digital bus for transporting PCM (Pulse Code Modulation) signals between telephony boards. It was created by the ECTF to provide a common bus structure for future development that would end the "bus wars" between the various legacy busses such as the SCbus and the MVIP bus.

PCM is a standard method of digitizing phone signals. It involves encoding each channel at an 8 kHz rate using eight bits. The signals from multiple channels are then combined into a frame. On the H.100 bus, each frame consists of 128 channels or timeslots. The bit rate of the H.100 bus is 8.192 MHZ. Thirty-two wires, also called streams, each carrying 128 timeslots, are combined to form the bus, and provide a total of 4096 timeslots. Two timeslots are required for a full conversation, one for each talker. For compatibility purposes with legacy busses, the first sixteen streams can also run at either 2.048 or 4.096 MHZ. with 32 or 64 timeslots respectively.

In addition to the streams, a number of other signals necessary to maintain synchronization between all the boards in the system are carried on the bus. These signals provide the clocking and framing information. Redundant clocks are provided to aid in recovery if the primary clock should fail. For interoperation with the SCbus, MVIP

bus, or H.MVIP bus a number of compatibility clock signals are also defined.

The H.100 bus consists of a 68 conductor ribbon cable that is used to interconnect the boards in the system. This cable connects to a header at the upper right hand edge on each board.

1.1.5 Clock Modes

The H.100 Loop Start Board can operate in a variety of clock modes. Modes are available so that the master clock can either be derived from the H.100 bus or be provided by an internal source on the H.100 Loop Start Board. The clock redundancy and clock fallback functions of the H.100 bus are also supported so that the H.100 Loop Start Board can be set to provide a clock to the H.100 if the master clock on that bus should fail.

1.1.6 Message Passing

The board occupies 8K of memory space on the host PC. This 8K may reside anywhere within the PC's address space. As a PCI board, the address and interrupt of the board is assigned at boot time. The message passing scheme used by the Infinity Series H.100 Loop Start Board is identical to that of the other Infinity Series H.100 boards, allowing for the easy combination of a variety of Infinity Series H.100 boards in a single system.

The message passing scheme and message syntax of Infinity Series H.100 boards is similar to that of the older XDS series of MVIP and SCbus boards. At the driver and API level, support is provided for both series of boards so that the H.100 boards may interoperate with legacy boards using a common interface.

1.1.7 Flash EAROM for Firmware

The firmware for both the main processors and for the DSP's is contained in Flash EAROM. This allows for easy upgrades of the firmware on the board in the field without requiring time consuming downloads every time a system boots. Once reprogrammed, the new firmware is retained even when the power is removed. The original, factory programmed firmware is also retained on board and can be accessed by installing a jumper.

1.1.8 Flash EAROM for Configuration Information

To reduce the burden on the application, the board has an EEPROM capable of providing non-volatile storage for configuration information. This information includes the port type, timing requirements, and the parameters necessary to conform to various national standards, supply voltages, etc. This configuration information, when saved, is automatically restored on a restart, allowing the board to automatically configure itself without host intervention.

1.2 How to Use This Manual

The first five sections in this manual are organized in the order you should read and use them to get started with your H.100 Loop Start Board. We recommend that you begin with these three steps.

1. Follow the instructions in section 2.0 (Quick Start) and 3.0 (Installation). These sections will tell you if your board is operating correctly within your system. You don't need to be familiar with the board's command set to complete this step.

2. Read section 4.0 (Initialization) to initialize the board within your system. Your application must perform these initialization procedures whenever you power-up your PC in order for the

board to communicate with the PC.

3. Read section 5.0 (Communications with the PC) for an overview of how to communicate with the H.100 Loop Start Board. Section 5.0 includes a summary of the commands for constructing your application and details concerning system interrupts.

Before you can actually build your application, read sections 6.0 (The H.100 Bus and Clock Modes) and 7.0 (Using the Loop Start board). These sections explain, with practical examples, how the H.100 Loop Start Board operates and how to use the command set to achieve the desired results. Section 8.0 explains diagnostic and error messages that may occur.

The Appendix contains information on power requirements and interfacing that will be helpful installing your H.100 Loop Start Board.

2.0 Quick Start

This section describes the first steps you should perform to determine if your Infinity Series H.100 Loop Start Board is communicating correctly with your PC system. You can perform this quick check without securing the board to the PC chassis or connecting any cables.

The exact procedure will vary depending on which operating system you are running. For each operating systems, drivers are required to interface to the boards. The drivers supplied by Amtelco have tests built into them to verify communications with the boards. These drivers also come supplied with utility programs that allow the developer to test communications with the board. Please consult the appropriate documentation for the driver and operating system you are using.

Quick Start Procedure

1. Make sure the PC power is off, then insert the board into a PCI slot.

2. Turn on your PC.

3. If the Amtelco driver is not already installed, install it now, following the instructions supplied with the driver.

4. Most Amtelco drivers will display a list of boards that are installed (see the documentation for the particular driver that you are using). If the H.100 Loop Start Board is listed, skip to step 6.

5. If the board is not listed, there may be a problem with the board not being seated correctly in the motherboard. There

may also be a problem with a memory or interrupt conflict. Power down the PC and check that the board is properly seated in the connector and repeat steps 1-4. If this does not remedy the problem, try removing any other computer telephony boards in the system. If your PC is unable to find the board, consult the number at the end of this section.

6. Run the program "xdsutil" supplied with the driver. Send the message "IN" to the H.100 Loop Start Board. The board should respond with the message "IA".

7. Send the message "VC" to the board. Verify that the Receive Message reads: `VCxxxxvvvvPLA` (where `xxxxvvvv` is a variable indicating the firmware version). Note that the 386 board will report as `PL`.

8. If the Communications screen shows the correct command responses, your H.100 Loop Start Board is communicating with the PC. You may now power down the computer and attach the necessary cables (see section 3.4)

For technical assistance, call Amtelco at 1-608-838-4194 ext.168.

3.0 Installation

This section describes how to install your Infinity Series H.100 Loop Start Board into your PC and how to use the jumpers, headers, and connectors. Before you begin the installation procedure, be sure to test the board as described in section 2.0 (Quick Start).

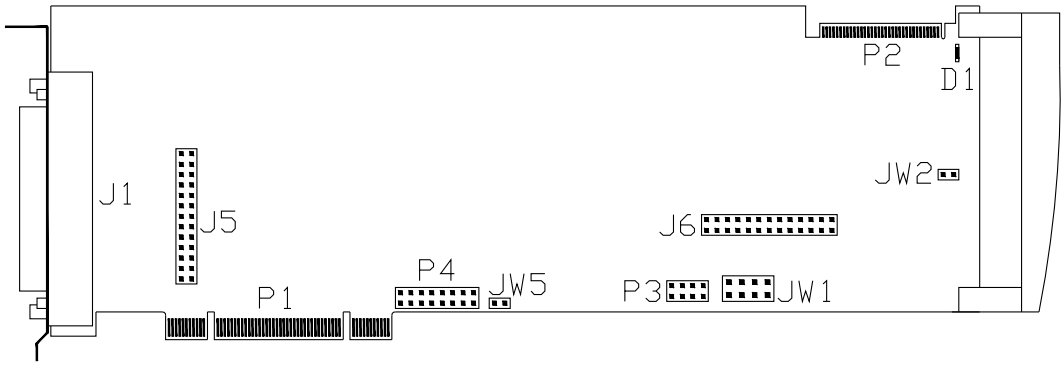

Figure 2: Location of Jumpers, Headers, and Connectors for boards with the 386 processor

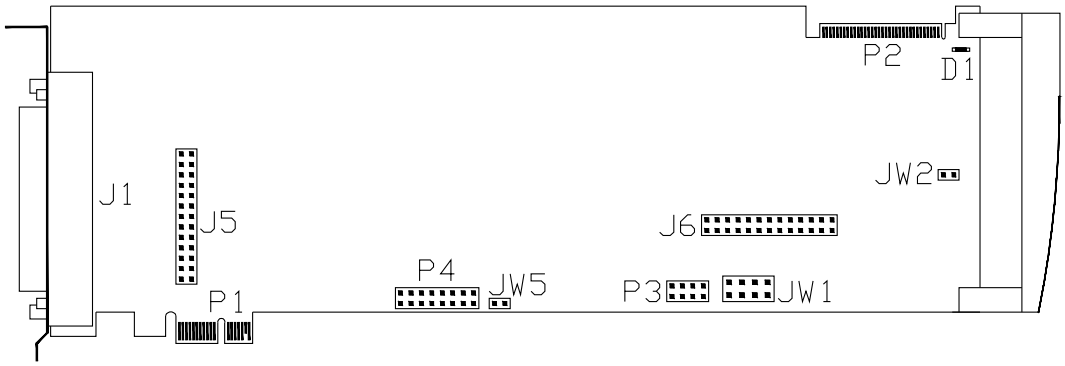

Figure 2a: Location of Jumpers, Headers, and Connectors for boards with the ARM processor

3.1 PCI Configuration

As Infinity Series boards conform to the PCI and PCI Express standards, there are no switches to set to configure the H.100 Loop Start Board's memory address, I/O addresses, or interrupt. The PC's bios will automatically configure the board at boot time to avoid conflicts with other boards in the system.

3.2 Jumpers & Headers

The following is a list of jumpers for the H.100 Loop Start Board:

JW1-1 Firmware Select. If firmware has been downloaded to the board, this jumper selects whether the downloaded firmware or the factory default firmware is used. When this jumper is installed, the factory default firmware is executed whenever the board is reset. When the jumper is not installed, the downloaded firmware will be executed after a reset if it is present. If no downloaded firmware is present, the factory default firmware is executed after reset.

JW1-2 Undefined, reserved for future use.

JW1-3 Reserved. This jumper should not be installed.

JW1-4 Undefined, reserved for future use.

JW2 DSP Firmware Select. Two separate firmware programs are included in the EAROM, one for the board processor and one for the DSP. If JW2 is installed and downloaded DSP firmware is present, the factory DSP firmware is executed after reset. Otherwise, the downloaded firmware is executed if present..

JW5 This jumper is used for factory testing and should not have jumpers installed.

J5, J6 Used to install a mezzanine board.

P3 Diagnostic port. Never install jumpers here.

P4 This header is used for programming internal logic and should never be jumpered.

3.3 Connectors: P2 and J1

P2 H.100 bus. The H.100 bus connector (P2) is a standard H.100 bus header. Use an H.100 bus ribbon cable to connect the H.100 Loop Start Board to other H.100 boards within the same PC chassis.

J1 Analog telephone connections. This connector is a standard RJ21 type 50 pin connector. It contains the audio pairs for both the base and daughter board. Each port occupies one pair in order. See Figure 3.

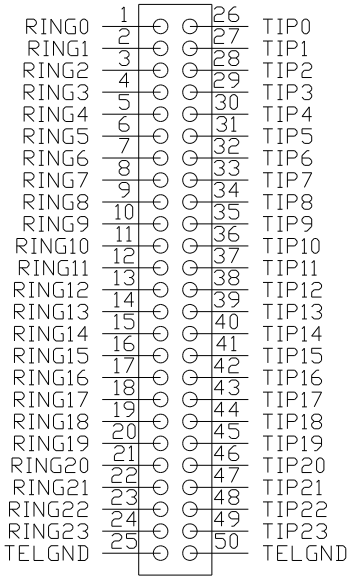

Figure 3: RJ21 J1 Pin Assignments

3.4 Installation

To install the H.100 Loop Start Board in your system:

1. Do not connect the board to the PSTN. Follow the quick check procedures described in section 2.0 to verify the operation of the board.

2. If the quick check is successful, turn off the PC power and remove the board from the chassis.

3. Install any necessary board jumpers. See section 3.2 for jumper configurations.

4. Reinsert the board into the chassis. Seat it properly in a PCI or PCI Express slot as appropriate in the PC chassis and tighten the screw in the back of the board to secure it. Do not connect the board to the PSTN.

5. Connect the H.100 cable to P2. Do not connect the telephony power supply to the PC.

6. Reinstall the PC cover. Connect the PC to the mains supply using a socket-outlet with protective earthing connection and connect any additional protective earthing used. Connect the telephony power supply to the PC.

7. Connect the telephone cable to J1. The telephone cable terminates in an RJ-21 male connector. Secure with mounting screws.

If it is subsequently desired to open the host equipment chassis for any reason, the PSTN cable and telephony power supply must be detached prior to effecting access to any internal parts which may carry telecommunications network voltages.

The PC chassis containing this device shall be placed in a secure location with access restricted to qualified service personnel.

3.5 Installing a Mezzanine Board

A mezzanine board is connected to the base board with a series of headers and attached with five posts and screws. To install a daughter board:

1. Place the base board component side up on a flat, non-conductive surface.

2. Position the mezzanine board component side down above the base board so that the headers align.

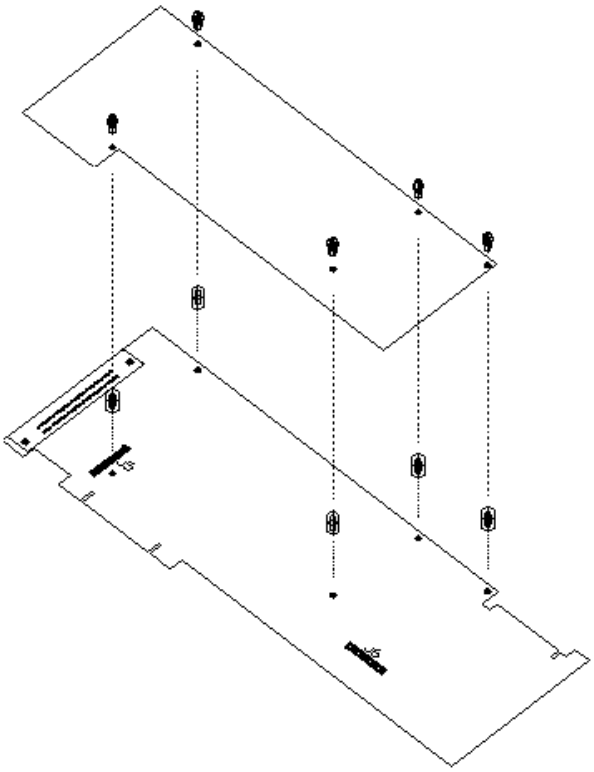

Figure 4: Installing a Mezzanine Board

3. Carefully insert the header pins in the mating base board connectors J5 and J6, being sure that none of the pins bend.

4. Fasten the five spacing posts with the provided screws to the base board.

4.0 Initialization

This section describes the procedures necessary to initialize the system and enable the PC to communicate with the Infinity Series H.100 Loop Start Board. XDS drivers will implement some of these procedures.

4.1 PCI Initialization

The system BIOS is responsible for recognizing PCI and PCI Express boards and mapping them into the I/O and memory spaces as required. It is also responsible for assigning interrupts to the board. This is done through a set of on board registers which contain information specifying the memory, I/O, and interrupt needs of the board. A set of BIOS functions exist for accessing this information. A detailed description of these functions can be found in the *PCI BIOS Specification* published by the PCI SIG, the PCI Special Interest Group.

Normally, the drivers supplied by Amtelco will take care of the process of finding Infinity Series boards and establishing communications. The information in the rest of this subsection is for background only.

The configuration registers of every PCI board contain a vendor ID and device ID code. These codes are unique to each board vendor. The vendor ID is 14E3h and the device ID is 0101h for the PCI version of the board. The device ID is 0301h for the PCI Express version. A BIOS function exists that will find each instance of a particular vendor and device ID, and which returns with a bus and device number. The bus and device number is then used in functions to read the configuration registers.

The configuration registers contain information on the base address of

the memory and I/O assigned to the board by the BIOS. A PCI board may have up to six different base addresses. On Infinity Series H.100 boards, the first two base addresses are used by the PCI bus interface logic. The third base address which is contained in registers 18-1Bh contains the memory location of the dual-ported memory that is used to pass messages. The interrupt information is contained in register 3Ch. The information in these configuration registers can be used by a driver to address the board.

4.2 Initialization Commands

The H.100 Loop Start Board is initialized by sending a sequence of command messages to the board. The process of sending messages is described in detail in Section 5.0, but normally it is accomplished either with a low-level driver XMT command or the API function **xds_msg_send.** Response messages are read using the low-level driver RCV command or the API function **xds_message_receive**.

To enable communications with the H.100 Loop Start Board, an **IN** command message should be sent to the board. The board will respond with an **IA** message.

The board may be reset using the command message **RA**. The board will respond with an **RA** message.

Your application can now configure the H.100 Loop Start Board using these commands

Command	Purpose
SCmsabb(c)	Sets the clock mode for the board. The parameter m is the clock-mode. The parameter s is the clock sub-mode. The parameters a, bb, and c are used to

specify additional clock control information such as compatibility modes, clock rates, local network, and CT_NETREF settings. The default mode on power-up or restart is mode 0. See section 6.0 of this manual for details of clock mode arguments.

SBabcd This command is used to define the clock rate for the lower 16 streams for compatibility with the SCbus or MVIP bus. The parameters a, b, c, d are used to set the rate for streams 0-3, 4-7, 8-11, and 12-15 respectively. The default value is 8.192 MHz. The possible settings are:

0 - 2.048 MHz., 32 timeslots per stream
1 - 4.096 MHz., 64 timeslots per stream
2 - 8.192 MHz., 128 timeslots per stream

SEx Sets the encoding mode for the board. The parameter x can be either M for Mu-Law as used in North America and Japan, or A for A-Law as used in Europe and Asia. The default value is for Mu-Law.

SHxxaabb Sets the parameters for hookflash and linebreak detection for port xx. The aa parameter is the minimum time for a hookflash to be detected in increments of .01 sec., bb is the maximum time. Any interruption in current longer than bb is considered a linebreak. If aa is greater than bb, hookflashes will not be detected. The default for these parameters is 340 and 330 msec. in keeping with North American standards for a linebreak and no hookflash detection.

SOxxabcde Sets the options o for port xx. Each option may be set to "Y" for yes, "N" for no, or '* for no change. The default is no. If option a is set to yes, an "SF" message will be sent if loop current is detected upon seizure of the loop. If option b is set to yes, changes in battery polarity will be reported with "Sr" and "Sn" messages. If option c is set to yes, the line will not be seized, but an audio path will be created when a connect or other command is issued. If option d is set to yes, the port will not disconnect upon the detection of a linebreak. If option e is set to yes, Caller ID is disabled.

ST(xx...xx) Set the port type for each port on the board. Port types can be "L" for loop start, or "N" or "U" for undefined for unused ports. An "*" may be used to indicate no change. The L type is used when interfacing to PSTN or PBX loop lines. The port type parameter must be included for each of the ports on the board.

STab Controls termination. Parameters a and b control termination for the H.100 and MVIP bus respectively. When set to E, termination is enabled and when set to D, termination is disabled. Boards on the end of the H.100 cable should have termination enabled. When operating in MVIP compatibility mode, the MVIP termination should be enabled when the following condition exists:

> For systems with five or fewer MVIP Bus connections and less than 90 pF load on the clock lines, it is adequate to place the circuit board that is the master clock source at one end of the cable and provide termination on the circuit board which is physically at the other end of the cable.

On systems with more than five MVIP connections or more than 90 pF load on the clock lines, both ends of the cable should be electrically terminated with the 1000 Ohm/1000 pF termination. No other boards should terminate these lines.

SXstt This command is used to set the base timeslot on the SCbus when reserving timeslots to transmit on. The parameters s and tt are hexadecimal numbers setting the lowest timeslot of the block of timeslots reserved for the board. This command should only be used when operating in the SCbus mode.

4.3 Configuration Memory

Much of the configuration information used to initialize the board is fixed in nature, such as the port types, options, and hook status timing. To simplify initialization of the board, the configuration can be stored in an onboard EEPROM. This information can be recalled upon a restart of the board eliminating the need to send this information to the board each time an application runs. To control the EEPROM, three commands are provided. These are:

SMS This command saves the current configuration information..

SML This command will cause the configuration saved in the EEPROM to be loaded into the processor memory. It is not necessary to use this command on a restart as the information saved in the EEPROM will automatically be loaded into the processor memory.

SMC This command will clear the EEPROM. If this command is used, the board will not read the EEPROM on a power up or restart and all required configuration information will have to be sent from the application.

If the board configuration is saved in Flash, it will still be necessary to send the **IN** and **SC** messages to enable messages and set the clock mode.

5.0 Communicating with the PC

This section describes how the PC communicates with the Infinity Series H.100 Loop Start Board. It includes the definitions for the H.100 Loop Start Board commands and responses along with a description of the mailboxes used for messaging.

The board is controlled by the host PC through a system of four mailboxes. The messages consist of short NUL-terminated ASCII strings, which are easy for the host software to compose and parse. The board is capable of buffering up to eight messages in either direction and can drive an interrupt line when it has a message for the host. Messages may not exceed 32 characters.

There are two main mailboxes, one for messages to the board and one for messages from the board, and two flags associated with them. A 00h in a flag byte indicates the mailbox is free, a non-zero value indicates that the mailbox is occupied. The mailboxes and their flags are contained in an 8K block of dual-ported memory at the following offsets:

receive mailbox	1F80h
transmit mailbox	1FC0h
transmit flag	1FFCh
receive flag	1FFEh

The board's base address is determined by reading PCI Configuration Space offset 18h. The 32-bit value at this location is the base address for the dual-ported memory on the board.

To send a message, the message is placed in the mailbox and the flag is set to 01h. To read a message, the message is removed from the mailbox

and the flag is cleared to 00h. This will clear the interrupt hardware.

5.1 Commands and Responses Protocol

This section describes the necessary step-by-step procedures for the PC to send a command to the board and to remove a response from the board.

5.1.1 Sending Commands to the Board

The basic steps to sending a command to the H.100 Loop Start Board are:

1. Build a command. Broadly speaking, a command is a string of ASCII characters with a NUL (00h) termination character.

2. Check the transmit flag. If the flag is 0, continue with the next step to put the command in memory. If the flag is not 0, wait until the flag is 0.

3. Insert the command in transmit mailbox memory beginning at the address of the transmit mailbox.

4. Write 01h to the transmit flag. This notifies the board that a message is waiting.

5.1.2 Reading Messages From the Board

1. Check the receive flag. If the flag is 0, there is no message. If it is non-zero, a message is waiting. Continue with the next step to read the message.

2. Remove the message from memory, starting at the address of the receive mailbox. Messages are NUL terminated ASCII strings.

3. Write 0h to the receive flag.

5.1.3 Reading Board Information

A range of board information is included in memory so that it can be checked without sending a message:

Type of Information	Offset Address
Board ID	1F00-1F03
Firmware Version	1F04-1F07
Processor Identifier	1F0F
Number of transmit timeslots	1F10-1F11
Base timeslot	1F12-1F13
Clock mode settings	1F18-1F1B
Board configuration	1F1C-1F1E
Clock status bits	1F1F
ID Code (serial number)	1F30-1F3F

Note: The number of reserved transmit timeslots, and base timeslots are used only in the SCbus compatibility mode when reserving transmit timeslots.

The board stores its identity upon power up or a hardware restart. The phrase **`Restart PLA (c) Amtelco 2007`** appears in the receive mailbox. On the 386 version of the board the phrase is **`Restart PL (c) Amtelco 2002`**. The receive flag is not set and no interrupt is generated.

5.2 Interrupts

The H.100 Loop Start Board can generate an interrupt to the PC indicating that a message is available. The interrupt for PCI boards is assigned by the BIOS or Operating System at boot time. The assignment is dependent on which PCI slot the board is in. The interrupt

line is usually shared by more than one device. If multiple Infinity Series boards are installed they may or may not all share the same interrupt line.

In order for an Infinity Series board to send interrupts to the PC, the PCI Interface circuit on the board must be programmed to enable interrupts. This is accomplished by setting bits 0 and 3 in the board's Interrupt Control/Status Register. This is a byte-wide register located at an offset of 69h from PCI Base Address 0. PCI Base Address 0 is contained in PCI Configuration Space register 10h. The Base address is a 32-bit value and is mapped into memory.

When an Infinity Series board sends a message, it generates a local interrupt to the PCI Interface circuit on the board. If the PCI Interface circuit has been programmed to generate interrupts to the PC, the local interrupt is passed through to the PC. When the PC receives an interrupt, its Interrupt Service Routine (ISR) should check the Infinity board's receive flag to see if a message is pending (i.e. the receive flag is non-zero). It should then process the message for the board and write a 0 to the board's receive flag.

5.2.1 Interrupt Initialization

1. Read and then clear the board's receive flag.

2. Read the PCI Base Address 0 from PCI Configuration Space offset 10h (this must be a 32-bit access).

3. Clear bits 0, 2, and 3 of PCI Base Address 0 + 4Dh. Clear bits 1 and 3 and set bits 0 and 6 of PCI Base Address 0 + 4C. Do not modify any other bits in this register. These registers are byte-wide memory mapped registers.

5.2.2 Step-by-Step Interrupt Processing Summary

1. Check to see if the receive flag is non-zero.

2. Remove the message from the receive mailbox.

3. Write 0h to the receive flag.

4. Re-enable the interrupt controller on the PC.

5.3 Commands and Responses

This section gives a general overview of the H.100 Loop Start Board commands and responses. The commands are grouped by function and then listed in alphabetical order by two-letter command. Refer to sections 6.0 through 8.0 for examples and explanations of how to use these commands.

5.3.1 Characteristics of Command Strings

- All commands consist of null (00h) terminated ASCII strings.

- There are no spaces or other delimiters between parameters in the commands.

- All letters in command strings must be UPPERCASE unless otherwise noted.

- Lowercase monospaced letters (such as `xx`) in the following command references represent parameters within commands. Each letter represents one ASCII digit.

- Numeric parameters are always hexadecimal numbers.

5.3.2 Command Parameters

The table below documents the common parameters for many of the commands listed in the next sections.

Common Command Parameters

Parameter	Definition	Values
xx	port number	00-17h
sstt	H.100 bus stream & timeslot number, ss = stream, tt = timeslot on stream	ss = 00-1Fh t = 00-7Fh
aabb	H.100 bus stream & timeslot number, aa = stream, bb = timeslot on stream	aa = 00-1Fh bb = 00-7Fh
bsstt	MVIP-95 terminus, b = bus ss = stream, tt = timeslot	b = H, L ss = 00-1F tt = 00-7F

5.3.3 Commands from the PC to the H.100 Loop Start Board

Note that section 7.0 of this manual provide supplemental information for the commands and messages documented here.

Port Commands

CAxxsstt Set port xx to listen to stream ss timeslot tt

CBxx Set port to hold if not busy, else return SBxx

CCxxssttaabb Connect port xx to stream ss timeslot tt and from stream aa timeslot bb

CDxx Disconnect port or call progress tone xx

CExxdd Enable energy detection for port xx, look for energy of duration dd

CExxF Disable energy detection for port xx

CFxxd Generate a hookflash on port xx for d tenths of sec.

CFxxdd Generate a hookflash on port xx for dd .01 sec.

CHxx Put port xx on hold

CIxx Disable output to CT bus

CLxx Set port xx to detect DTMF digits, play dial tone

CLxxo Set port xx to detect DTMF digits, option o
F - turn detection off
M - monitor mode, maintain existing connections
Q - regular mode, suppress dial tone

CMxx Enable audio for port xx, no switching or control

CPxxy Give port xx call progress tone y where y values are

0 - dial tone	6 - European dial tone
1 - reorder	7 - congestion tone
2 - busy	8 - European busy tone
3 - audible ringback	9 - European ringback
4 - Digital Milliwatt	A - U.K. ringback
5 - silence	B - Japanese ringback

CSxxsstt Play call progress tone to stream ss timeslot tt, xx values 20-2Bh correspond to progress tones 0-B

CTxx(ds) Send dial string ds to port xx, valid tones in string are: 0-9, *, #, A-D, U - upper tone (941 Hz.), L - lower tone, (697 Hz.), X - short pause, P - long pause, N - North American dial tone, E - European dial tone, a-i, special & programmable tones

CVxxffffllffffllnnffrr Generate custom tone on port xx
ffff = freq. 1st & 2nd tone, ll = level 1st & 2nd tone
nn = on duration, ff = off duration, rr = repetitions

CWxxD Disable Call Waiting detection on port xx

CWxxE Enable Call Waiting detection on port xx

CXxxsstt Set port xx to transmit on stream ss timeslot tt

CZxxD Disable Echo Suppression on port xx

CZxxE	Enable Echo Suppression on port xx
CZxxX	Enable External Echo Suppression on port xx

Interrupt Control Commands

IN	Enable transmit interrupts and messages
IF	Disable transmit interrupts and messages

MVIP Compatibility Commands

MDhhD	Disable DTMF detector hh (MVIP) (00-1F)
MDhhE	Enable DTMF detector hh (MVIP) (00-1F)
MEhhdd	Enable Energy detector hh (MVIP) (00-1F) duration dd
MEhhF	Disable Energy detector hh (MVIP) (00-1F)
MGhh(ds)	Generate the dial string (ds) with generator hh (MVIP) (00-1F)
MMxxD	Disable Music on Hold input for port xx
MMxxE	Enable Music on Hold input for port xx
MObssttD	Set_output disable mode, bsstt - output terminus
MObssttEbsstt	Set_output enable mode, bsstt - output terminus, bsstt - input terminus
MObssttPpp	Set_output pattern mode, bsstt - output terminus, pp - pattern value
MTD	Disable output to the CT Bus (tristate)
MTE	Enable output to the CT Bus (tristate)

Query Commands

	(the QH command applies only to ARM boards)
QHHsstt	Query T8105, sstt = H.100 stream and timeslot
QHLsstt	Query T8105,sstt = local stream and timeslot
QHR00rr	Query T8105, rr = control resgister address
QObsstt	Query Output for terminus bsstt
QPdx(msg)	Send message to DSP d, send only bits 0-3 of x
QXxxx	Query SCbus transmit timeslot for Port xxx

Reset Commands

RA	Reset all (resets ports, DSP functions, H.100 bus)
RD	Reset DSP (resets DSP chip only)
RPxx	Reset port xx

Setup Commands

Saxxmttmrr	Set AGC for port xx, m = mode A - AGC, + - positive gain, - - negative gain; tt = transmit gain, rr = receive gain in .5 dB steps
SBabcd	Set bit rate for streams 0-3, 4-7, 8-11, and 12-15 0 - 2.048 MHz. 1 - 4.096 MHz. 2 - 8.192 MHz.
SCmsabb(c)	Set clock mode m submode s, arguments a, bb, & c
SDttffffllffffllnnff	Set custom dialed digit tone tt ffff = freq. 1st & 2nd tone, ll = level 1st & 2nd tone; nn = on duration, ff = off duration
SEa	Set Encoding mode a, M = Mu-Law, A= A-Law
SHxxaabb	Set hookflash/linebreak times for port xx aa = minimum time, bb = maximum time > bb is a linebreak
Sittffffllffffllnnffnnff	Set custom information (call progress) tone ii ffff = freq. 1st & 2nd tone, ll = level 1st & 2nd tone; nn = 1st & 2nd on duration, ff = 1st & 2nd off duration.
SMC	Clear the EEPROM configuration contents
SML	Load the EEPROM contents onto the board
SMS	Save the configuration in EEPROM
SOxxabcd	Set options for port xx, Y for yes, N for no, * no change
ST(xx...xx)	Set port types for each port where x values are: L - Loop Start N - No type defined U - Undefined/unused * - No change to port type

STab	Set bus termination, a = H.100 bus, b = MVIP bus
SXstt	Set SCbus base timeslot to stream s, timeslot tt
SX	Clear Scbus base timeslot setting

Version Requests

VA	Checksum of alternate segment request
VC	Version request
VD	DSP version request

Download Commands

@xxxx	Download 1K block to address xxxx
@Es	Erase segment s
GA	Jump to Alternate Program
GM	Jump to Main Program
GZ	Jump to Diagnostic Monitor
@R	Read in Alternate Program to 10000h
@WA	Write Alternate Program to Flash
@WD	Write Main Program to Flash
@WF	Write Main Program to Flash except for boot code

5.3.4 Responses from the H.100 Loop Start Board

Acknowledgments

IA	Acknowledge interrupts enabled
RA	Reset all acknowledged
RD	DSP Reset acknowledged
RPdd	Reset port dd acknowledged
SMx	EEPROM operation x = 0 - failure, 1 success

Caller Identity Messages

DDxxdate/#	Caller Identity date and number detected on port xx
DNxx<name>	Caller Identity name detected on port xx

Error Messages

ECxx	Clock error bit xx

Query Responses

(note the QH response applies only to ARM boards)

QHHssttllllcsttttttdddd	Reply to T8105 H.100 bus query, llll - location, cstt - stream, timeslot, control & valid bit, tttt - tag, dddd - data memory
QHLssttcsttdd	Reply to T8105 local bus query, cstt - source stream, timeslot, & control, dd - data memory
QHR00rr	Reply to T8105 register query, rr - reg. dd - data
QObssttm(bsstt)	Query_output reply, bsstt - output terminus, m - mode, (bsstt) input terminus
QPd(text)	DSP diagnostic responses from DSP d
QXxxxstt	SCbus transmit timeslot for port xxx
QXxxxZ	No SCbus transmit timeslot set for port xxx

Port State Change Messages

SBxx	Port xx is busy (response to CBxx message)
SCxx	Connect on port xx acknowledged
SExx	Tone string on port xx completed
SEXhh	Tone string from generator hh ended
SFxx	Port xx off-hook
SHxx	Hold on port xx acknowledged
SIxx	Disconnect on port xx acknowledged
SLxx	Listen on port xx acknowledged
SMxx	Audio enable on port xx acknowledged
Snxx	Battery polarity normal on port xx
SNxx	Port xx on-hook
SPxxr	Energy detection on port xx, r = 1 energy detected, r = 0 energy ended
SPXhhr	Energy detector hh results r
SQxx	Hookflash detected on port xx
Srxx	Battery polarity reversed on port xx
SRxx	Ring detected on port xx

STxxd	DTMF digit d detected on port xx
STXhhd	DTMF digit d detected by detector hh (MVIP)
SWxx	Call Waiting detected on port xx
SXxx	Transmit on port xx acknowledged

Diagnostic Responses

VAxxxx	Checksum of the alternate segment
VCxxxxyyyyPLA	Version response, xxxx = checksum of main segment, yyyy = version number, PLA = board type, (PL on 386 boards)
VDxxxx	DSP version xxxx
U(msg)	An undefined or unparseable message response

6.0 The H.100 Bus & Clock Modes

The Infinity Series H.100 Loop Start Board provides a means of connecting analog Loop Start lines to the digital H.100 computer telephony bus. Through this bus, the Loop Start lines can be connected to other H.100 compatible boards. To accomplish this, the board has complete access to all streams and timeslots on the bus. It is capable of operating in a variety of clock modes compatible with H.100 operation. In addition, the board is capable of interoperating with legacy MVIP and SCbus boards.

6.1 The H.100 Bus

The H.100 bus consists of 32 Pulse Code Modulation (PCM) streams operating at an 8.192 MHZ. clock rate. Each stream contains 128 timeslots, for a total of 4096 timeslots. In addition to the PCM data signals, there are a number of bit, frame, and network reference signals that are used to synchronize the operation of multiple boards. For interoperation with the legacy SCbus, MVIP-90 bus and the H-MVIP bus there are some additional clock signals that are included on the bus.

For the purposes of commands, a particular H.100 timeslot is referred to by a four digit hexadecimal number. The first two digits are the stream number, while the last two digits are the timeslot within the stream. Streams range from 00h to 1Fh, and timeslots from 00-7Fh.

The physical H.100 bus is a 68 conductor ribbon cable that connects the various boards in the system. As in any such bus, termination is important for its proper operation. The board at each end of the H.100 cable must have the proper termination installed or enabled, while any board between the ends must not terminate the bus. For the H.100 Loop

Start Board, termination is enabled using a command of the form **STab** where a controls the H.100 termination and b the MVIP bus termination. Termination is enabled if a is "E" and disabled if a is "D".

6.1.1 Legacy Bus Compatibility

The H.100 specification provides for inter-operability with several common legacy PCM busses. These include the SCbus, the MVIP-90 bus and the H-MVIP bus. Because these busses run at different bit rates than the 8.192 MHZ. of the H.100 bus, provisions exist in the specification to run the first 16 streams at either 4.096 MHZ. or 2.048 MHZ. For inter-operability with the SCbus, these streams typically should be run at 4.096 MHZ. (2.048 MHZ. and 8.192 MHZ are also possible choices) and with the MVIP-90 bus they should be run at 2.048 MHZ. H-MVIP runs these streams at either 2.048 or 8.192 MHZ. depending on whether MVIP-90 compatibility is desired.

On the H.100 Loop Start Board, the bit rate of the first 16 streams is set using the "SB" command. This command takes the form **SBabcd** where the parameters a, b, c, and d select the bit rate for streams 0-3, 4-7, 8-11, and 12-15 respectively. The choices for these parameters are:

0 - 2.048 MHZ.
1 - 4.096 MHZ
2 - 8.192 MHZ.

Thus to operate with the SCbus at 4.096 MHZ. the command would be **SB1111** and to operate with the MVIP-90 bus **SB0000**. The default selection for these streams is the H.100 rate of 8.192 MHZ.

When operating in a compatibility mode, the timeslot in board commands range from 00 to the maximum number of timeslots allowed by the bit rate. At 2.048 MHZ. timeslots within a stream are numbered 00-1Fh and at 4.096 the timeslots are 00-3Fh. MVIP bus streams are numbered 00-0Fh. This numbering corresponds to the DSo/DSi

convention according to the following table:

H.100 stream	MVIP-90 stream	MVIP-95 stream	H.100 stream	MVIP-90 stream	MVIP-95 stream
00h	DSo0	HDS0	08h	DSo4	HDS8
01h	DSi0	HDS1	09h	DSi4	HDS9
02h	DSo1	HDS2	0Ah	DSo5	HDS10
03h	DSi1	HDS3	0Bh	DSi5	HDS11
04h	DSo2	HDS4	0Ch	DSo6	HDS12
05h	DSi2	HDS5	0Dh	DSi6	HDS13
06h	DSo3	HDS6	0Eh	DSo7	HDS14
07h	DSi3	HDS7	0Fh	DSi7	HDS15

6.2 Clock Modes

The H.100 bus specification defines a variety of clock signals. Two clock signals CT bus A and CT bus B are provided for redundancy. In addition, a signal called CT_NETREF is defined which may be referenced to an external clock source such as a T1 or E1 span. This signal exists to aid in recovery if the primary clock source should fail. The specification also includes clock signals for compatibility with both the MVIP-90 and SCbus.

The clock mode must be set before any connections can be made with other boards. The clock mode is set using the Set Clock command "SCmsabbc", where m is the clock mode, s is the sub-mode, and a, bb, and c are additional arguments used to select clock sources and specify compatibility modes. The default clock mode on a power up is to provide a local clock, but to neither source clock signals to the bus or derive the clock from the bus. The possible clock modes are:

0 no clocks to or from the bus
1 clocks slaved to the CT bus
2 the board is clock master CT bus clock A
3 the board is clock master CT bus clock B
4 the board is secondary master for CT bus clock A
5 the board is secondary master for CT bus clock B

Connections are possible only when all boards within a system are synchronized to the same clock. Only one board in a system can provide the H.100 bus clock. The other boards in the system must slave their internal clocks to the master. If the H.100 Loop Start Board is to use the H.100 bus clock, this clock must be provided by another board before switching can be accomplished.

6.2.1 Slave Mode

In the Slave Mode, the H.100 Loop Start Board derives its clocks from one of the clock signals on the CT bus. The clock signal is selected with the submode argument in the **SC** command. The possible clock signals are:

0 - CT bus clock A
1 - CT bus clock B
2 - SCbus clock at 2 MHZ.
3 - SCbus clock at 4 MHZ.
4 - SCbus clock at 8 MHZ.
5 - MVIP-90 clock signal
6 - CT bus clock A, auto-fallback mode
7 - CT bus clock B, auto-fallback mode

Argument a is used to set the CT_NETREF mode, while argument bb is used to select the source of CT_NETREF. The choices for argument a are:

0 - No CT_NETREF output
1 - CT_NETREF output is enabled

As the H.100 Station Board does not connect to any external digital networks, only the no CT_NETREF output selection is valid. The CT_NETREF source is specified by argument bb, and should always be set to 00.

6.2.2 Primary Master Mode

In modes 2 or 3, the board supplies the CT master clocks A or B respectively. Other boards on the H.100 bus will synchronize to one of these clocks. The source of the clock is selected by the submode argument s. The choices are:

0 - freerun, the board's internal clock
1 - CT_NETREF

For submode 1 and 2, argument bb will select the frequency of the CT_NETREF signal. The choices is:

00 - 8 kHz. (frame rate)

Note that on earlier boards other CT_NETREF rates were supported, but that this is not possible with the switching chip used on this board.

Submode 0 should only be chosen if there are no other boards in the system that can derive clocks from an external digital network.

For all modes, argument a will select the legacy bus compatible clocks that the board will supply. The options are:

0 - no compatibility clocks
1 - SCbus clocks at 2 MHZ.
2 - SCbus clocks at 4 MHZ.
3 - SCbus clocks at 8 MHZ.
4 - MVIP 90 clocks
5 - H-MVIP clocks

6.2.3 Secondary Master Modes

When a board is operating as a secondary master, it uses the other clock signal as a source, i.e. if a board is the secondary master for CT clock B, it uses CT clock A as a source and provides CT clock B. If the primary clock fails, the secondary master then becomes the clock master. Typically, one board will be set as the master for clock A and another board as the secondary master for clock B, or vice versa. If the clock source specified by the submode is either of the CT_NETREF signals the board will automatically fall back on that source if the primary clock source should fail. If set to free-run, it will fall back to a PLL that was locked to the primary master clock.

In all secondary master modes, if the primary master fails, the board will automatically become the new primary master. If the original primary master is restored, the clock mode for the original secondary master must be reset.

When operating in secondary master mode, the arguments s, a, and bb are the same as when operating as a primary master.

6.2.4 Clock Fallback

The H.100 Specification details a scheme for automatically recovering from a clock failure. One of the CT bus clocks, either A or B is designated the master clock. The other clock is the secondary master and is generated by a different board than the primary clock. While the

primary clock is valid, the secondary clock is locked to it. If the primary clock should fail, the secondary clock takes over using a local oscillator, CT_NETREF, or a local network as the source. Boards that are slaves should automatically fall back to the secondary clock. After a failure of the master clock, system software should designate new primary and secondary clocks. The new primary may be the previous secondary clock master. For Infinity Series H.100 boards, this will involve sending a set clock command with the new primary clock information.

When an Infinity Series board is set for automatic fallback, the board will automatically switch to the secondary clock if the primary clock fails. When this occurs, the board will send an "EC" message indicating the failure. When the application designates a new primary master, it should send a new clock mode command to the board even though auto-fallback may have occurred.

6.2.5 Clock Errors

If the board detects a problem with the clocks, it will generate a clock error, which notifies the application that it should take appropriate action. Clock errors are reported in the Clock Error Bit message, **ECxx** where the **xx** is a hexadecimal value in which each bit identifies the specific error. A value of 1 indicates an error condition. The bits are as follows:

bit	Error Description
0	CT bus clock A
1	CT bus clock B
2	SCbus clocks
3	MVIP bus clocks
4	CT_NETREF error
5	Frame Boundary

6.3 Configuration Information

Information on the clock mode setting, stream rates, and other configuration settings is available in the dual-ported memory in an eight byte block beginning at an offset of 1F18h. The first four bytes are the clock mode, the submode, and the a and bb arguments from the set clock command **SC**. The next byte contains the stream rate information from the **SB** command with bits 0-1 containing the value for streams 0-3, bits 2-3 for streams 4-7, and so on. Bits 0 and 1 of the sixth byte indicate the state of the H.100 and MVIP termination, respectively, with a value of 1 being the enabled state. The seventh byte will always be 0 for the H.100 Loop Start Board as the board can not derive clocks from an external network. The eighth byte contains the clock error status bits. These are in the same order as in the **EC** clock error message (Sec. 6.2.5).

7.0 Using the Loop Start Board

This section describes the process used for controlling the ports on the Infinity Series H.100 Loop Start Board. The steps necessary for configuring a board will be described. Basic functions such as making a connection, detecting ringing, playing call progress and DTMF tones, and detecting DTMF tones and energy will be described. Additional features such as detecting Caller Identity information will also be explained. Examples of making incoming and outgoing calls combining several functions are included.

7.1 Overview of the Command Structure

The command set described in this section are called the "C" Commands. Each of these commands instructs the board to take all the actions necessary to perform a function such as making a connection, playing a tone, or detecting DTMF digits. Thus, the command to detect DTMF digits will play dial tone to the port, connect it to a DTMF detector, and activate that detector.

Many of the commands use a common form for the various arguments. The port number is usually the first argument, and will be between 00 and 17 (00 and 0B if no mezzanine board is included).

The arguments used to define the source or destination consist of a four digit hexadecimal number. The first two digits are used to indicate the stream. There are 32 streams defined on the H.100 bus and these range from 00 to 1F. The last two digits are used to indicate the timeslot. H.100 streams have 128 timeslots ranging from 00-7Fh. As an example, the argument **712** would refer to stream 7, timeslot 12h, or 18 decimal.

7.2 Legacy Computer Telephony Busses

The H.100 bus specifications make provisions for connecting to legacy computer telephony busses such as the SCbus and the MVIP bus. When interoperating with the SCbus or MVIP bus, the first 16 streams are used for connecting to the legacy bus, and these streams may operate at less than the 8.192 MHZ. bus rate. This means that there will be fewer than 128 timeslots per stream.

7.2.1 SCbus Compatibility

The SCbus is a 16 stream bus. Each stream on the bus normally operates at 4.096 MHZ. and has 64 timeslots per stream for a total of 1024 timeslots. However, the SCbus may optionally run at either 2.048 MHZ. with 32 timeslots per stream for a total of 512 timeslots or 8.192 MHZ. with 128 timeslots per stream and a total of 2048 timeslots on the 16 streams. When inter-operating H.100 Loop Start Board with the SCbus at either 2.048 or 4.096 MHZ. the bit rate on the lower 16 H.100 streams must be set appropriately using the "SB" command.

The SCbus uses a 26 conductor ribbon cable. Because of this, an adapter must be used between the P2 connector on the H.100 board and the SCbus.

7.2.2 SCbus Timeslot Assignment

Typically, drivers and libraries conforming to the SCbus specification use a scheme called "timeslot assignment" to insure that no two devices are transmitting on the same timeslot. Not only will having two transmitters on the same timeslot degrade audio signals, but they also may damage some SCbus boards. To prevent this, each device or "port" is assigned a unique timeslot to transmit on during boot-up.

Transmit timeslots are reserved on the H.100 Loop Start Board using the

"SX" command. The same command is used to reserve timeslots on XDS SCbus boards. The command takes the form **SXstt** where s is the stream and tt is the timeslot on that stream of the timeslot reserved for the first port on the board. As an example, if the first timeslot reserved for the board is 100 in decimal, then the message **SX124** would be sent (timeslot 100 corresponds to stream 1, timeslot 24h).

When timeslots have been assigned, the actual output timeslot value is no longer used in commands that control outputs to the CT bus. Instead, the port number is used. This port number will range from 0 to 31 and will be represented in stream timeslot notation (0stt) in the commands. In this notation, the ports will run from 0000-0017.

Normally, the timeslot assignment process is carried out as part of the initialization and loading of the driver. A configuration file is used to specify the number of timeslots to be reserved for the board. The function **xds_xmt_timeslot** is used for finding the transmit timeslot of a port. To aid this process, information on the number of reserved timeslots and the base timeslot is presented in the dual-ported memory. This information is available at the following locations:

1F10h	total number of timeslots for the board
1F12h	1st timeslot assigned to the board

The command **QXstt** can also be used to inquire as to which timeslot is reserved for a port stt. The reply takes the form **QXsttabb** where a is the stream and bb is the timeslot on the stream that is reserved for stt. If no timeslots have been reserved on the board, the response will take the form **QXsttZ.**

7.2.3 MVIP Compatibility

The MVIP-90 bus has 16 streams with 32 timeslots each. The streams run with a bit rate of 2.048 MHZ. When the H.100 Loop Start Board is inter-operating with he MVIP bus, the bus rate on the lower 16 streams

must be set using the "SB" command.

The MVIP-90 bus uses a 40 pin ribbon cable. To connect the H.100 Loop Start Board to the MVIP-90 bus an adapter must be used. The MVIP rules for termination must also be followed (see Section 4.2).

Timeslots on the MVIP bus are normally paired, that is timeslot x on DSoy is paired with timeslot x on DSiy. One timeslot of a pair must be defined as an input and the other as an output. With most MVIP boards, an attempt to use both timeslots of a pair as inputs or as outputs will result in a conflict. The table in Section 6.1.1 gives the association between H.100 stream numbers and the DSi and DSo streams.

MVIP-90 applications normally assign timeslots dynamically. Connections that are not enabled are tri-stated. As only one source may drive a timeslot on the CTbus, it is important that any connection to a timeslot be disabled before a new connection is made to that timeslot.

The H-MVIP bus has 24 streams. The H-MVIP specification has several modes. One mode is compatible the MVIP-90 specification, that is the lower 16 streams run at a 2.048 MHZ. rate while streams 16-23 run at 8.192 MHZ. This mode can be treated as the MVIP-90 case. In another mode, all 24 streams run at the same 8.192 MHZ. rate as the H.100 bus. In this case, only the physical cabling between the H-MVIP bus and the H.100 bus and clock issues need to be addressed.

7.2.4 MVIP Compatibility Commands

Several commands exist for compatibility with the MVIP-95 driver specification. This specification uses the concept of a "terminus" to define an input or output timeslot. The terminus argument consists of three parts, a bus, a stream within the bus, and a timeslot on that stream. In MVIP compatibility messages, a terminus is represented by a five character string. The first character indicates the bus. Valid bus selections are "H" for the H.100 CT bus, and "L" for the local bus. The

local bus provides connections to the analog ports and DSP resources as shown in the following table:

Local Stream	Input	Output
0	ports 00-17	ports 00-17
1	voice ports 00-1F	voice ports 00-1F
2	none	call progress tones 0-1B
3	DTMF & Energy detectors 00-1F	DTMF generators 00-1F

In the MVIP compatibility mode, connections are controlled using the Set Output command **MO**. This command takes the form **MObssttm**, where "bsstt" is the output terminus being controlled, and m is the mode. Valid modes are "D" for disable, "E" for enable, and "P" for pattern output. In the enabled mode, the input terminus follows the mode character, and in the pattern mode, a two digit hexadecimal number representing the value of the byte to be output follows the mode. As an example, the message "MOH0123EL0000" would enable a connection from port 00 to the H.100 timeslot 23h, stream 1. Connections can be made between the H.100 bus and the local bus, or between timeslots on the local bus. Under some circumstances, it may be necessary to issue a **CMxx** command to enable audio if the port is not set to type "L" or "N".

In the MVIP compatibility mode, additional commands are needed to control the DSP resources. The DTMF detectors are controlled with a command of the form **MDhhm** where hh is the detector number or handle and m is the mode, either "D" to disable or "E" to enable the detector. When a detector is enabled, detected digits are reported in a message of the form **STXhhd** where hh is the detector number and d is the digit. The Energy detectors are controlled with a command of the form **MEhhdd** where hh is the detector number and dd is the minimum

duration of the signal to be detected in .1 second increments. To disable an energy detector, the command takes the form **MEhhF.** To generate DTMF digits the command takes the form **MGhh(string)** where hh is the generator and "string" is the string of DTMF digits. This string may include pauses. Completion of the string is indicated by a message of the form **SEXhh** where hh is the generator number. To access the DSP resources, a "MO" Set Output command must be issued to connect the resource to the desired port or H.100 timeslot as well as issuing the resource control command. It is the responsibility of the application to manage the DSP resource in the MVIP compatibility mode.

As an example of detecting digits in the MVIP compatibility mode:

commands	responses	description
MOL0000EL0200		connect port 00 to dial tone
MOL0301EL0000		connect DTMF detector 1 to port 00
MD01E		enable DTMF detector 1
	STX011	digit 1 detected
MOL0000D		disable dial-tone
	STX012	digit 2 detected
	STX013	digit 3 detected
MOL0301D		disable input to detector 1
MD01D		disable DTMF detector 1

A query command **QObsstt** is also available to query the state of the output terminus "bsstt". This command corresponds to the Query_Output command in the MVIP-95 specification. The response takes the form **QObssttm(bsstt)** where "bsstt" is the output terminus, "m" is the mode, and if the mode is enable, the second "bsstt" is the input terminus.

7.3 Configuring the Board

Several steps are necessary when configuring the board. The most important item is to select the clock mode. Only one board in the system can generate the Master Clock. If available, an E1, T1, or Primary Rate ISDN board should serve as the master. If no such board exists in the system, and one or more Basic Rate ISDN ports configured as a terminal equipment interface is connected to the public switched telephone network, then one of these ports should be the source of the master clock. (See Sec. 6.2 for clock mode details)

The clocks must be configured before any switching can take place. It should be noted that boards on the SCbus may fail to operate unless a master clock is provided, therefore, when inter-operating with SCbus boards, it may be necessary to configure the clock on the H.100 Loop Start Board before trying to download software or issue commands to other boards on the SCbus. It is also important that the board providing the master clock be configured **last** after all other boards have had their clock modes set. This is required for the proper operation of the SC2000 chip used to interface to the SCbus on most SCSA boards.

Several other steps may be necessary to configure individual ports. A port can be configured as unused or undefined, a network termination, or as terminal equipment. The **"ST"** command is used to configure the ports. It consists of characters, one for each port, representing the port type. An "L" defines a port as a loop start port, and an "N" or "U" as undefined or unused. A loop start port is used to interface to a PSTN or PBX loop line that uses ringing or hook status to signal for call control. As an example, if the first eight ports are to operate as loop start ports and the rest as unused ports, then the "ST" message to be sent would be:

STLLLLLLLLUUUUUUUUUUUUUU

If no mezzanine board is installed, only 12 port type characters would need to be sent.

There may be situations because of loop length where it is desirable to add gain or attenuation to a port. This can be done with a command of the form **SAxxpttprr** where xx is the port number, p is the polarity of the gain and tt and rr are the gains. The polarity can be either a "+" or a "-". The gain is specified in .5 dBm steps with a range from -20 to + 20 dBm. For example, the command "SA00+06-06" would add +3 dBm gain in the transmit direction and -3 dBm gain in the receive direction on port 00.

The port type and gain information can be stored in the Flash memory to be loaded automatically on power up or a restart. See Section 4.3 for details.

7.4 Using the "C" Commands

The analog ports on the H.100 Loop Start Board can be set to provide full-duplex connections as well as half-duplex connections in either direction. They can also be used to send DTMF and call progress tones as well as provide DTMF and energy detection.

Changes in the port state are reported in state change messages. These consist of the letter "S" followed by a letter indicating the change, the port number, and an optional information character. An example is the message **SI00** which indicates that port 00 has returned to the idle state.

7.4.1 Making a Connection

A two-way connection can be made with a port using the Connect Command **"CC"**. This command takes the form **CCxxssttaabb**, where xx is the port number, sstt is the destination stream and timeslot and abb is the source stream and timeslot to be connected to. As an example, the message **CC0001020304** would connect port 00 with timeslot 2, stream 1 being the transmit timeslot and timeslot 4, stream 3 the receive timeslot. Note that if a transmit timeslot had been reserved for the port

using the "SX" command or if this had been done by a timeslot assignment program associated with a driver, the transmit timeslot portion of this command will be ignored and the reserved timeslot will be used. In addition to two-way connections, one-way connections are also possible in either direction. The Audit command **"CA"** is used to create a connection from a timeslot to a port. This command takes the form **CAxxsstt**, where xx is the port number, ss is the stream, and tt the timeslot of the timeslot being audited. As an example, **CA000201** would direct timeslot 1 of stream 2 to port 00.

The Transmit command **"CX"** is used to setup a port to transmit towards the H.100 bus. This command takes the form **CXxxsstt** where xx is the port number, ss is the stream and tt is the destination timeslot. As an example of using a port as an input, if port 01 is to transmit on timeslot 5 of stream 6 the command **CX010605** would be sent.

A Hold or other port command, such as playing a call progress tone, will also break a connection. The Hold command **"CHxx"** will disable audio to and from the port but not release the loop seizure. If the port was connected to the H.100 bus, a silence pattern will be output to the H.100 bus. This pattern can be disabled by a **"CDxx"** or **"CIxx"** command. It will also be cleared if a connect command is issued for the port. As only one source may drive a timeslot on the CT bus, it is important that any connection to a timeslot be disabled before a new connection is made to that timeslot.

All of the commands described above will result in a loop seizure unless the third port option is set to "Y".

A connection will be broken by a Disconnect command. The Disconnect command **"CDxx"** will release the loop seizure and disable the port output and any H.100 bus connection. An idle state change message **"SIxx"** will signal that the port has returned to the idle state.

7.4.2 Call Progress Tones

The on-board DSP can be used to play any of the standard Call Progress tones to a port. The tones supported are dial tone, busy tone, reorder tone, and audible ringback. Silence and a calibration tone of 1004 Hz. can also be played. A set of tones compatible with ETR 187 is also provided for use in Europe along with several ringback formats. Four additional custom tones (C-Fh) are also available. The Call Progress command **"CP"** is used to play tones. This message is of the form **CPxxt**, where xx is the port and `t` is the code of the tone. For example, the command **CP002** will play busy tone to port 00. The tone will stop playing if another command is issued for the port such as a connect.

The **"CS"** command may be used to play any one of the 16 tones to the CTbus for use on other boards. This command takes the form **CSxxsstt** where xx is the tone number in the range 20-2Fh, ss is the stream number and tt is the timeslot number. To disable the tone, the **"CD"** command is used with a port number in the range 20-2Fh.

7.4.3 Sending DTMF Tones

A string of DTMF tones can be sent using the **"CT"** command. Any of the 16 DTMF tones can be sent. Pauses may be embedded that are one or ten digit times (.2 or 2 sec.) Single tones of 697 and 941 Hz. are also possible. The tone string length can be up to 27 characters long. The command consists of **CT** followed by the port number and the string of tones. As an example, the command **CT039P7654321** would send the digit "9", pause two seconds, and then send the digits "7654321". This command will also result in a loop seizure.

On receiving the command, the board will respond with an **"SL"** state change message to indicate that the port is listening to a DTMF generator. When the tone string has finished, the board will send an **"SE"** message to indicate the string is ended and place the port in the

hold state.

7.4.4 Detecting DTMF Tones

The on-board DSP can be used to detect DTMF tones on a port. The Listen for DTMF command takes the form **CLxxo**, where xx is the port number and o is an option. If no option is given, dial tone will automatically be played to the port until the first tone is detected. If the option is "Q", then no dial tone will be played. If the option is "M", then detection will take place without interrupting existing connections. The "F" option will disable detection that is in progress. This command will also result in a loop seizure. As an example, the message **CL00** will enable DTMF detection on port 00 and play dial tone.

As each tone is detected, the board will send a Tone detected state change message of the form **STxxd** where xx is the port number and d is the tone. As an example, the message **ST005** indicates that the digit 5 has been detected on port 00. All sixteen DTMF tones can be detected. Detection will remain active until a command is issued for the port.

7.4.5 Detecting Energy

Each port is equipped with an energy detection function. The energy detector can be set to look for audio energy with a minimum duration time. When a continuous audio signal has been detected for that time, a message is sent. Another message is sent when the audio signal stops. This feature can be used to monitor for dial tone restoration or call progress tones. Energy detection does not affect existing connections and can be used in conjunction with DTMF detection.

To enable energy detection on a port the energy command **"CE"** is used. This command takes the form **CExxdd** where xx is the port number and dd is the duration in steps of 100 msec. The range is from .1 to 22.3

seconds or from 01 to DF. For example, the command **CE0714** would enable energy detection on port 7 with a duration of 14h or 2 seconds. When a signal is detected the message would take the form **SP071** in this example where the "1" indicates detection. A "0" would indicate that the signal has stopped.

Energy detection will be disabled when the port changes state due to a command. It can also be disabled without affecting the port state by sending a command where the duration is replaced by a single character "F". In the example above, this would be **CE07F**.

7.4.6 Detecting Ringing

When on hook, ports will detect ringing signals applied by the PSTN or PBX. This ringing may be of any frequency, voltage, or cadence as specified in the various national standards. Each time a ring is detected, the board will respond with a message of the form **SRxx** where xx is the port number. Filtering is included so that "split ring" signals that consist of two or more short bursts of ringing separated from the next ring cycle by a longer interval are only reported once per ring cycle.

7.4.7 Polarity Detection

Some PBXs use a polarity reversal to signal a disconnect. This may be detected if the second line option for a port is set to "Yes". If this is done, a change to reverse polarity will be indicated by a message of the form **Srxx** where xx is the port number. A return to normal polarity is indicated by a message of the form **Snxx**. Note that it is the responsibility of the application to act on these signals.

7.4.8 Hook-Flash and Linebreak Detection

Some equipment can generate a short interruption of current. This is normally used as a linebreak or disconnect signal, though it may also be

used to get the attention of the controlling software for special purposes such as initiating a call control function. When used in this manner it is called a hookflash. Interruptions less than a minimum time will be ignored, interruptions longer than a maximum duration will be considered a linebreak and interruptions with a duration between these two times will be considered a hook-flash.

The timing of the linebreak or hook-flash signal may vary with switch type and country. To allow for these variations, the hook-flash timing can be changed on a port by port basis. This is done with a command of the form **"SHxxaabb"** where xx is the port number, aa is the minimum time and bb is the maximum time for the hook flash in 10 msec. increments. On-hook signals of less than the minimum time will be ignored, those that are greater than the maximum will be treated as a disconnect. For example, the message **"SH00284B"** would set the minimum time for port 00 to 400 msec. and the maximum time to 750 msec. If the minimum time is greater than the maximum time, hook-flashes will not be detected. The default times is set to the North American standard of a 330 msec. linebreak time and no hookflash detection. These timing parameters may be saved in Flash memory.

If a linebreak is detected for an active call, it will be disconnected, that is the line will be released and the audio path will be cleared. A state change message of the form **"SNxx"** will be sent, where xx is the port number. This action may be set by setting line option d to yes. When a hook-flash is detected a message of the form **"SQxx"** is generated where xx is the port number. The application can then take appropriate action. It should be noted that when a hook flash is detected, the board takes no other action other than sending the message.

7.4.9 Hook-Flash Generation

Many loop start lines from the PSTN or PBXs can detect short on-hook intervals that can be used to get the attention of the controlling software for purposes such as initiating a transfer or answering a waiting call.

This is called a hook-flash, a term that derives from the hook switch on the hand set cradle of a telephone set. The Loop Start Board can generate a hook-flash using a command of the form **CFxxdd** where xx is the port number and d is the duration of the on-hook signal in increments of .01 seconds. For compatibility with older boards this command may also take the form **CFxxd** where the increments are in tenths of a second. In North America, hook-flash signals are typically in the range .5-.7 seconds, but this may vary with different PSTN or PBX equipment. In Europe, the pause is typically shorter, about .1 sec.

7.4.10 Caller Identity

The H.100 Loop Start Board is capable of detecting Caller Identity information to appropriately equipped Loop Start sets. This information includes the time and date of the call and the calling party number. The calling party name may also be included. For new calls, the information is normally sent between the first and second ring. The information may also be sent after a call waiting tone if another call is already in progress. The board will automatically look for caller identity information between the first and second ring. To detect the information when off-hook, the detector must be enabled with a command of the form **CWxxE** where xx is the port number.

Caller identity information, which includes the time, date, and number is normally sent between the first and second ring. When recieved, a message of the form **"DDxxmmddhhmm/#"** is sent by the board, where xx is the port number, mmdd is the month and date, hhmm is the hour and minute, and # is the calling party number. The date and time are in decimal using a 24 hour format.

The calling party name may be added to the information with a response message of the form **"DNxxname"** where xx is the port and name is the calling party name. The board will accept up to 28 characters in the name field, but current standards are limited to either 15 or 21 characters.

As an example of receiving caller identity information:

response	description
CR001	first ring detected
DD0004030201/6085551234	April 3, 2:01 AM, 608-555-1234
DN00John Smith	calling party name “John Smith”
CR001	second ring detected

Caller Identity information is sent using the Multiple Date Message Format (MDMF) format.

7.4.11 Automatic Gain Control

The H.100 Loop Start Board is equipped with an Automatic Gain Control (AGC) function through the on-board DSP. The AGC can control either the transmit or receive direction or both. It is also possible for the AGC circuit to supply a fixed amount of gain or loss in either or both directions.

The AGC function is controlled using the **“SA”** command. Each port can be controlled independently. Gain or loss in the fixed mode is available in .5 dB steps over a range of +/- 20 dB. This command takes the form **“SAxxmttmrr”** where xx is the port number, m is the mode, and tt and rr are the gain parameters for the transmit and receive directions respectively. The mode settings can be “A” for AGC on, “+” for positive gain, and “-” for negative gain. The gain parameter is specified in .5 dB steps as a two digit hexadecimal number in the range 00-28.

7.4.12 Echo Suppression

Echo Suppression may be enabled on a per port basis. When activated, it will compare the audio signal in the transmit and receive directions and suppress the receive signal if certain conditions are met. Echo suppression towards the H.100 bus is enabled with a command of the

form **CZxxE** where xx is the port number. Echo suppression towards the port is enabled with a command of the form **CZxxX.** Once enabled, echo suppression may be disabled using a command of the form **CZxxD**.

7.4.13 Music on Hold Inputs

Ports on the H.100 Loop Start Board can be used to input music on hold sources onto the H.100 bus. This usage converts the port into a high impedance input and does not involve the use of external transformers or the need to apply a voltage to the port. The command to enable this feature has the form **MMxxE** where xx is the port number. The connection is then made using the "MO" command. To disable the feature, the command takes the form **MMxxD.** Note that this feature does not use the internal state machine for ports. Using any of the "C" commands when the feature is enabled will disable the feature and may introduce other undesirable side effects.

7.5 Examples

This section gives detailed example of various situations typical of the operation of the board. The command and response messages are listed as well as a brief description of each step.

7.5.1 An Example of a Port Originating a Call

The following is an example of the steps involved in a port originating a call. Both the "C" commands and state change messages will be shown. First the port will be seized with a "CB" command which checks the port to see if its idle and seizes it if it isn't. A number will then be dialed and the connection made upon completion. The call will then be disconnected.

commands	responses	description
CB06		check to see if port is idle
	SH06	port seized
CT066085551212		send digit message
	SL06	DTMF generator set up
	SE06	digit string completed
CC0601020304		connect the port
	SC00	connection confirmation
CD06		disconnect the port
	SI06	port returned to idle state

7.5.2 An Example of a Port Receiving a Call

This example shows the steps involved in a Loop Start port receiving a call. First, ringing will be detected, then the port will be connected, and finally disconnected.

commands	responses	description
	SR06	ringing detected message
	SR06	second ring detected
CC0601020304		connect audio to the port
	SC06	connection confirmation
CD06		disconnect the port
	SI06	port in idle state

7.5.3 An Example of a Hook-Flash

This example shows what might happen if a Loop Start port uses a hook flash to get the attention of the application to perform some action such as transferring a call. The hook flash will be received, digits will be detected and then processed.

commands	responses	description
CF006		generate .6 sec. hook flash
CE0002		set energy detector to detect dial tone
	SP001	energy from dial tone detected
CT005551212		number dialed
	SL00	dialing begins
	SE00	dialing ends
CC0001000200		new connection made
	SC00	connection confirmation

7.5.4 An example of DTMF Detection

In this example, after ringing is detected, the DTMF detection will be enabled to collect digits from the caller.

commands	responses	description
	SR00	ringing detected
CL00		DTMF detection enabled with dial tone
	SX00	DTMF detection enabled
	ST001	the digit “1” is detected
	ST002	the digit “2” is detected
	ST003	the digit “3” is detected
CC0001000200		the caller is connected
	SC00	connection confirmation

7.5.5 An Example of Caller Identity Information

In the following example, Caller Identity information is detected between the first and second rings. After connection, Caller Identity Detection is enabled for Caller ID on Call Waiting.

commands	responses	description
	SR00	1st ring detected
	DD0001020304/5551212	date, time, and number
	DN00John Smith	calling name
	SR00	2nd ring
CC0001000200		connect command
	SC00	connect acknowledge
CW00E		caller id detection enabled
	SW00	call waiting signal
	DD0001020306/5551234	new calling #
	DN00Jane Jones	new calling name
CF007		hook flash to connect to 2nd caller

7.6 Voice Resources

The H.100 Loop Start Board is equipped with 32 channels of voice record and 32 channels of voice playback capability. The operation of these channels is beyond the scope of this document. For further information consult the appropriate driver and library manuals for the operating system you are using.

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8.0 Diagnostics & Error Messages

8.1 Diagnostic Commands

Several diagnostic commands are available:

VA Used to request the checksum of the firmware in the alternate segment of the board. This is returned in a message of the form `VAxxxx` where `xxxx` is the checksum of the firmware in the alternate segment of ROM.

VC Used to request the version of the firmware on the board. A message of the form `VCxxxxyyyyPLA` is returned, where `xxxx` is the checksum of the firmware stored in the main segment of ROM, `yyyy` is a four-digit version number, `PLA` indicates the board type (Loop Start Board, ARM Processor). This message takes the same form with all Infinity Series boards, and can be used to determine the configuration of the system. Note that the board ID is `PL` for boards with the 386 processor.

VD Used to request the version of the DSP software. This is returned in a message of the form `VDxxxx`, where `xxxx` is the version number. All DSP's on the board use the same software version.

QHbsstt Queries the T8105 switching chip, for bus `b`, stream and timeslot `sstt`. The bus value b can be either "H" for the H.100 bus or "L" for the local bus, or "R" for control registers. For the H.100 bus, the contents are returned in a message of the form `QHHssttllllcsttttttdddd`,

where `llll` is the connection memory location, cstt are the control bits, stream and timeslot and valid bit, `tttt` is the connection memory tag, and `dddd` is the contents of data memory 1 and data memory 2. If the timeslot is not found, only a location value of `01FF` is returned. For the local bus, the results are returned as a 24 bit value `csttdd` in a message of the form `QHLssttcsttdd`, where `cstt` is the source stream and timeslot, and `dd` is the data memory contents. The register results are returned as an 8 bit value in a message of the form `QHR00rrdd` where `rr` is the register address and `dd` is the data. This command refers to the details of the internal switching circuitry, and is ordinarily of limited use to an application. Note that this diagnostic is not applicable to boards with the 386.

QXxxx Queries the transmit timeslot reserved for port `xxx`. This command is only valid if the board is operating in SCbus mode. The reply takes the form `QXxxxstt` where `stt` is the stream and timeslot for the port. If no timeslot is assigned, the reply will be `QSxxxZ`. This command is common to all Infinity Series boards operating in the SCbus mode and all XDS SCSA boards. While the port number has three digits to allow for boards with up to 1024 channels, only the values 000 through 017 are valid for the H.100 Loop Start Board.

8.2 Error Messages

The board will detect a number of error conditions and respond with appropriate error messages. These messages are:

ECxx A clock error bit event `xx` has occurred. The value xx is a hexadecimal number where the bits are (a bit value of 1 is an error)

bit	description
0	CT bus clock A
1	CT bus clock B
2	SCbus clocks
3	MVIP bus clocks
4	CT_NETREF error
5	Frame Boundary

SM0 An EEPROM operation has failed. This indicates that either a read or write to the EEPROM was unsuccessful.

SM1 An EEPROM operation successfully completed.

U*[cmnd]* If the board does not recognize a command message, or if it does not have the appropriate number of arguments, the same message will be returned by the board preceded by a U to indicate an undefined message.

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Appendix A: Environmental Specifications

The Infinity Series H.100 Loop Start Board meets the following environmental specifications:

TEMPERATURE EXTREMES:

Operating: 0°C (+32°F) to +50°C (+122°F).
Storage: –40°C (–40°F) to +70°C (+158°F).

AMBIENT HUMIDITY:

All boards will withstand ambient relative humidity from 0% to 95% non-condensing in both operating and storage conditions.

MECHANICAL:

All Infinity Series H.100 boards conform to the PCI-SIG mechanical specifications for full-length PCI or PCI Express cards.

MTBF:

50,000 hours.

ELECTRICAL REQUIREMENTS:

+5 volts ±5% @ 1.5 amps maximum.
-5 volts, +3 volts, and ±12 volts are not required.

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Appendix B: Custom Tones

The DSP firmware provides a wide variety of dialed and information tones that should cover the majority of situations. However, for those cases when the standard set of tones is not sufficient, it is possible to modify these tones to provide custom capabilities.

The standard set of informational or call progress tones consist of the 12 tones listed in the table below. These tones can be played to a loop start line using the **CP** command. Any one of these twelve tones plus four additional tones may be modified by using the **SI** command to create a custom call progress tone. However, if this is done to one of the standard tones, the original tone will no longer be available.

Standard Call Progress Tones

tone	description	tone	description
00h	dial tone	06h	ETSI dial tone
01h	reorder	07h	congestion tone
02h	busy tone	08h	ETSI busy tone
03h	ringback	09h	ETSI ringback
04h	digital milliwatt	0Ah	U.K. ringback
05h	silence	0Bh	Japanese ringback

The command to create a custom call progress tone takes the form

SIttffffllffffllnnffnnff

where tt is the number of the tone, ffff are the first and second frequencies used to make the tone, ll is the level of the first and second frequencies in -dBm, and nn and ff are the on and off times of the tone in 50 msec. increments. To create complex cadences, a second on and off time may be specified. The freqeuncy range is from 0000-0CFFh or 0 to 3327 Hz. The levels ll of the two frequencie components is given in -dBm and has a range of 00-3Eh or 0 dBm to -62 dBm. A value of 3Fh will disable the frequency allowing a single frequency tone to be created. The on and off times are specified in 50 msec. increments and have a range of 00-FEh or 50-12700 msec. A duration of value of 0FFh will cause a continuous tone.

As an example, the command **SI04028A0A01A40A05050000** will change the digital milliwatt (tone 04) to a tone composed of the frequencies 650 and 420 Hz. each at -10 dBm with a cadence of 250 msec. on and 250 msec. off.

Custom tones can also be created for use with the **CT** command. The standard set of tones consists of 30 tones plus a tone that is reserved for custom programming as given in the following table. The first 16 tones are the standard DTMF tones. The next four tones are used to provide a lower and upper single frequency tone and a short and long pause. The next nine tones are used for the Call Waiting and Caller ID functions. The last standard tone is a "bong" tone for alerting users. Tone 1Eh is available for customization.

Any of these 31 tones may be customized using the **SD** command, however if one of the standard tones is modified, it is no longer available. It is therefore not recommended that the standard tones (00-1Dh) be modified if it can be avoided. The form of the command to modify a tone is:

SDttffffllffffllnnff

where tt is the tone, ffff is the first and second frequencies used to make

the tone, ll is the level of the first and second frequencies, and nn and ff are the on and off durations of the tone. The on and off times are specified in 10 msec. steps and have a range of 00h-FFh or 10 to 2550 msec. The ranges for the other arguments are the same as for the **SI** command.

Standard Dialed Digit Tones

Tone	Char.	Description	Tone	Char.	Description
00	0	DTMF 0	10	L	697 Hz.
01	1	DTMF 1	11	U	941 Hz.
02	2	DTMF 2	12	X	.2 sec pause
03	3	DTMF 3	13	P	2 sec. pause
04	4	DTMF 4	14	N	dial tone
05	5	DTMF 5	15	E	ETSI dial tone
06	6	DTMF 6	16	a	440 Hz. .1/.1
07	7	DTMF 7	17	b	440 Hz. .1/.03
08	8	DTMF 8	18	c	440 Hz. .3/.1
09	9	DTMF 9	19	d	440 Hz. .3/.03
0A	A	DTMF A	1A	e	2130/3750 Hz. .08
0B	B	DT MF B	1B	f	2130/3750 Hz. .1on/.05 off
0C	C	DT MF C	1C	g	DTMF D .06 on/0 off
0D	D	DTMF D	1D	h	.5 sec. “bong”
0E	*	DTMF *	1E	i	user tone
0F	#	DTMF #	1F		unavailable

As an example, to modify the first user programmable tone, the command **SD1D028A0A01A40A0505** would create a tone composed of the frequencies 650 and 420 Hz. at -10 dBm with an on and off duration of 250 msec. To send this tone to a port, the command would be **CT00h.**

It is also possible to send a custom tone on a one time basis to a specific port. The command to do this takes the form:

CVxxffffllffffllnnffrr

where xx is the port number, ffff and ll are the frequencies and levels of the first and second tone as in the commands above, nn and ff are the on and off durations of the tone pair, and rr is the number of times the tones repeat. the on and off times are specified in 50 msec. steps and have a range of 00-50h or 0 msec. to 4.0 sec. The number of repetitions ranges from 01-FFh. If a value of 00h is used, the digit will be played one time. The frequencies and levels have the same ranges as for the SI command.

As an example, the command **CV04028A0A01A40A050507** would send a tone consisting of 650 and 420 Hz. at -10 dBm, on and off durations of 250 msec. and repeating a total of seven times to port 4.